IN THE CLAIMS

Please substitute these amended claims in the application. Marked-up versions showing additions underlined and deletions in brackets are attached at Appendix A.

1. (Amended) A differential controlled delay unit, comprising:

a first amplifier having a first and a second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor is connected to a drain of the second transistor and a gate of the second transistor is connected to a drain of the first transistor; and

a second amplifier having a third and a fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals, wherein a differential input voltage is connected to gates of the second amplifier transistors, and a control input and power supply voltage is connected to sources of the first amplifier.

10. (Amended) The voltage controlled oscillator of Claim 7, further comprising an additional delay unit.

11. (Amended) The voltage controlled oscillator of Claim 7, wherein the transistors for the first amplifiers are PMOS and the transistors for the second amplifiers are NMOS and a drain of the first and second transistors is connected to a drain of the third and fourth transistors to form outputs of the delay units.

12. (Amended) The voltage controlled oscillator of Claim 11, further comprising an additional delay unit.

13. (Amended) The voltage controlled oscillator of Claim 7, wherein in the first delay unit and the second delay unit, drains of the first amplifier are connected to drains of the second amplifier to form output terminals.